Claims:

1. A polishing pad useful for planarizing semiconductor substrates, the polishing pad comprising a polymeric material having a porosity of at least 0.1 volume percent, a KEL energy loss factor at 40 °C and 1 rad/sec of 385 to 750 1/Pa and a modulus E' at 40 °C and 1 rad/sec of 100 to 400 MPa.

2. The polishing pad of claim 1 wherein the KEL energy loss factor at 40 °C and 1 rad/sec is 395 to 700 1/Pa.

3. A polishing pad useful for planarizing semiconductor substrates, the polishing pad comprising a polymeric material having a porosity of at least 0.1 volume percent, a KEL energy loss factor at 40 °C and 1 rad/sec of 405 to 600 1/Pa, a modulus E' at 40 °C and 1 rad/sec of 140 to 300 MPa and a Shore D hardness of 20 to 60.

4. The polishing pad of claim 3 wherein the polymeric material is polyurethane and the polymeric material has a density of 0.5 to 1.05 g/cm^3.

5. The polishing pad of claim 4 wherein the polyurethane has a cross-linked structure.

6. A polishing pad useful for planarizing semiconductor substrates, the polishing pad comprising a polyurethane polymeric material having a porosity of at least 0.1 volume percent, the polyurethane polymeric material being formed from a prepolymer reaction product of toluene diisocyanate and polytetramethylene ether glycol with 4,4'-methylene-bis-o-chloroaniline and the prepolymer reaction product having a 6.7 to 8.6 weight percent NCO and an NH_2 to NCO stoichiometric ratio of 80 to 110 percent.

7. The polishing pad of claim 6 wherein the prepolymer reaction product has a 7.05 to 8.5 weight percent NCO.

8. The polishing pad of claim 6 wherein the polishing pad comprises a polymeric material having a porosity of at least 0.1 volume percent, a KEL energy loss factor at 40 °C and 1 rad/sec of 405 to 600 1/Pa, a modulus E' at 40 °C and 1 rad/sec of 140 to 300 MPa and a Shore D hardness of 20 to 60.

9. A method of polishing a semiconductor substrate including the step of polishing the semiconductor substrate with a polishing pad useful for planarizing semiconductor substrates, the polishing pad comprising a polymeric material having a porosity of at least 0.1 volume percent, a KEL energy loss factor at 40 °C and 1 rad/sec of 385 to 750 1/Pa and a modulus E' at 40 °C and 1 rad/sec of 100 to 400 MPa.

10. The method of claim 9 wherein the semiconductor substrate is a patterned wafer and the polishing pad polishes the patterned wafer.